



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,130	09/08/2003	Thoai-Thai Le	10808/94	5405
48581	7590	03/09/2005	EXAMINER	
BRINKS HOFER GILSON & LIONE INFINEON PO BOX 10395 CHICAGO, IL 60610				LAM, DAVID
		ART UNIT		PAPER NUMBER
		2827		

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,130	LE ET AL.	
	Examiner David Lam	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on amendment file on 12/02/04.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-30 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 16-20 is/are allowed.
 6) Claim(s) 1-5,10-12,21,26 and 28-30 is/are rejected.
 7) Claim(s) 6-9,13-15,22-25 and 27 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 1/05, 2/05.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1- 5, 10, are rejected under 35 U.S.C. 102(e) as being anticipated by Mes (6,539,454).

Regarding to claims 1-5, 10, Mes discloses a memory device comprising: a DRAM, a delay-locked loop circuit (DLL, CLK-IO) receives an external clock signal, and having a plurality of delay elements; a synchronization circuit (60, 61) coupled to the delay-locked loop circuit and a synchronization enable signal (64), the synchronization circuit outputting a plurality

of enable signals (LATCH-ENX); an output circuit having a buffer (pipe latch 1-3, 58) coupled to a data input enable signal and a data output enable signals, the buffer circuit generating an output (32); a read circuit (50) having a signal sense array, wherein the synchronization circuit provide first and second read enable signals (IODB_READX).

Regarding to claims 11- 12, Mes discloses a memory device comprising: a DRAM, a delay-locked loop circuit (DLL, CLK-IO) receives an external clock signal, and having a plurality of delay elements; a synchronization circuit (60, 61) coupled to the delay-locked loop circuit and a synchronization enable signal (64), the synchronization circuit outputting a plurality of enable signals (LATCH-ENX); a read circuit (50, 52, 54) having a signal sense amplifier coupled to the synchronization circuit and receive a read enable signal from the synchronization circuit.

With regard to claims 21, 26, 28-30, they encompass the same scope of invention as to that of claims 1- 5, 10-12, except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Allowable Subject Matter

2. Claims 13-15, 22-25, 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the above noted output circuit further comprises a data input

pointer coupled to receive a data input enable signal and a data output pointer circuit coupled to receive a data output enable signal. Method reading according to independent claims 21, 26 and further comprising step of generating a plurality of delayed clock signal based upon the external clock signal.

3. The following is an examiner's statement of reasons for allowance: Claims 16-20 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach: a memory device comprising a synchronization circuit, among others as claimed in independent claims 16, 20, coupled to a delay-locked loop circuit and receiving a plurality of delay clock signals and a synchronization enable signal, and output a data output enable signal.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Miki (6,552,955) discloses a semiconductor memory device with reduced power consumption.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam



DAVID LAM
PRIMARY EXAMINER

March 5, 2005